



## Knowledge Inn (in nature). 19

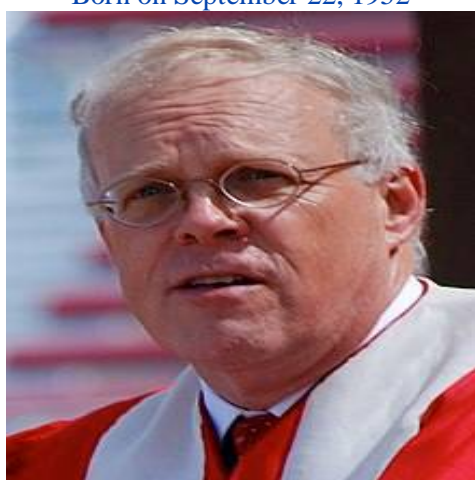
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### Research Profile of John L. Hennessy

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John L. Hennessy  
Born on September 22, 1952



At Huntington, New York, U.S.

	All	Since2016
<u>Citations</u>	45,210	6049
<u>h-index</u>	69	22
<u># Papers</u>	600+	

#### Biological Family of John L. Hennessy

Father	Aerospace engineer	
Mother	Teacher before raising her children	
Wife	Andrea Berti	Married in 1974



**(deemed Nobel Prize for Computing)**

**Of year 2017 goes to**

**Two collaborators  
John Hennessy (left), David Patterson (Right)**




**for their work pioneering an approach (RISC) to computer architecture and its impact on the microprocessor industry**




### Response of Hennessy on receiving Turing award

- ! The Turing Award is truly a capstone to my career as a computer scientist
- ! I am honored to join many previous winners of the award and they happen to be my Stanford colleagues, namely Don Knuth, Ed Feigenbaum, John McCarthy, and Martin Hellman
- ! It feels good to be part of that group of awardees of Turing prize
- ! “To be with august body, it’s kind of a touch of immortality,”
- ! This award also celebrates (both informal and formal) collaborations between me and Dave Patterson (professor emeritus of computer science at the University of California, Berkeley) for about 30 years,
- ! “It’s maybe a smaller version of winning the Nobel Prize,”

### Open heart expression of Hennessy

- ! Prof. Hennessy acknowledges that there were gaps in his skill set when he addressed audience as president of Stanford
  - ➔ For instance “I had never given a speech that didn’t include visual aids”
- ! Don’t think you’re the smartest person in the room.  
 Don’t think you have all the answers for queries in the range boson to Universe
  - ? This is humility
- ! I’m a computer scientist,” he says, chuckling, “and the powers of two are very important, so the next one after 16 is 32.”
- ✓ For us, “Turing award is s a capstone,” Hennessy said
- ✓ Our careers are pretty much shaped at this point
- ✓ We aren’t expecting any big career advancements

### Hennessy- teaching

-  I do teach. I’m teaching a freshman seminar “Great Discoveries and Inventions in Computing.”
-  It’s sort of a survey of all the interesting things that have happened in the computing field over time, from hardware to software,
  -  I’ve got 16 bright-eyed, bushy-tailed students.

### Appreciations for Hennessy’s sparking intellect

Charles Prober<sup>#</sup>, a friend, marvels at lock-trap memory of unnerving capacity of Hennessy’.

-  Prober says” “Hennessy summons details from a book he read years earlier”

📖 while “he himself sometimes forgets details from a book while still reading”

Marc Andreessen called him "the godfather of Silicon Valley” 102 check

# senior associate dean for medical education at the School of Medicine

### Academic profile of John Leroy Hennessy

Hennessy was a tinkerer in high school	Won a science fair prize for an automated tic-tac-toe machine
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1973	Bachelor's degree	Electrical engineering	Villanova University
1975	M Sc	Computer science	Stony Brook University (then S.U.N.Y. Stonybrook)

Ph.D.	Computer science	Stony Brook University	1977
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Ph.D Thesis	A real-time language for small processors: design, definition and implementation
Doctoral advisor	Richard Kieburtz

Doctoral students	<ul style="list-style-type: none"> <li>✓ Anant Agarwal</li> <li>✓ Lawrence Paulson</li> <li>✓ Josep Torrellas</li> </ul>
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### Employment. John Leroy Hennessy

1977-83	Assistant Professor	Electrical engineering	Stanford
1983-86	Associate Professor		Stanford
1984	Sabbatical year	Founded MIPS Computer Systems Inc	----
1986-present	Willard and Inez Kerr Bell Endowed Professor–inaugural holder	Electrical Engineering and Computer Science	Stanford

### Academic administrative positions

1989–93	Director	Stanford's Computer System Laboratory#	Stanford
1994–96	Chair	Department of Computer Science	Stanford
1996–99	Dean	School of Engineering	Stanford

#: research center run by Stanford's Electrical Engineering and Computer Science departments

<b>Administrative ladder in Academic institute</b>		
1999-2000	Provost	o Stanford
2000-2016	President	o Stanford
2016-present	Director Knight-Hennessy Scholars Program <sup>&amp;</sup>	o Stanford o
Board member	Google (later Alphabet Inc) -- chair of the board CISCO Systems Atheros Communications Gordon and Betty Moore Foundation	

<b>Knight-Hennessy Scholars Program &amp;</b>	<ul style="list-style-type: none"> <li>✓ In 2016, Hennessy co-founded the Knight-Hennessy Scholars program</li> <li>✓ Hennessy was its inaugural Shriram Family Director</li> <li>✓ The program has a \$750 million endowment</li> <li>✓ This programme fully funds graduate or professional degree students in any of Stanford's seven schools for up to three years</li> <li>✓ The inaugural class of 51 scholars from 21 countries joined at Stanford in the fall of 2018</li> </ul>	
	➔ Focus	Experience will be both in Knowledge and Leadership development
	➔ Goal	<b>!</b> Preparing a new generation of leaders <ul style="list-style-type: none"> <li>o To enforce a positive impact on the world</li> </ul>

<b>RISC (Reduced Instruction Set Computer)</b>		
1981	John Hennessy David Patterson	<b>!</b> Revolutionized computing <ul style="list-style-type: none"> <li>+ Increasing performance</li> <li>+ Reducing costs</li> </ul>
1984	Hennessy	<ul style="list-style-type: none"> <li>✓ Cofounding MIPS Computer Systems</li> <li>✓ Helped transfer this technology to industry</li> <li>✓ Chief Scientist, (1984-1992)</li> </ul>
1989	Initial public offering	
1992-1998	Hennessy	<ul style="list-style-type: none"> <li>✓ Chief Architect, Silicon Graphics Computer Systems</li> </ul>
1998	Hennessy	<ul style="list-style-type: none"> <li>✓ Cofounded Atheros Communications               <ul style="list-style-type: none"> <li>+ A pioneer in wifi technology</li> </ul> </li> <li>✓ Chair of the Board; 1998- 2010</li> </ul>

Books of John Leroy Hennessy

Year	Title	Authors
	Computer Organization and Design Hardware/Software Interface	John Leroy Hennessy David A. Patterson
	Computer Architecture: A Quantitative Approach, fifth edition	

A few Awards <a href="#">John Leroy Hennessy received</a>	
1983	o John J. Gallen Memorial award by Villanova
1984	o Presidential Young Investigator, National Science Foundation
1997	o Fellow, Association for Computing Machinery
2000	o John Von Neumann Medal (jointly with D. Patterson), IEEE
2012	o IEEE Medal of Honor
2017	o Fellow of the Royal Academy of Engineering, United Kingdom
2020	o BBVA Foundation Frontiers of Knowledge Award
2020	o Clark Kerr Award
	Honorary Doctorate Degrees 17
2010 Oct14	o 14th Dalai Lama presented a khata

Judge for Awards	
2013	➔ Member of panel of judges for the inaugural Queen Elizabeth Prize for Engineering
2015 to 2017	➔ Continued

## Research papers of John Leroy Hennessy

TITLE	CITED BY	YEAR
<a href="#">Computer architecture: a quantitative approach</a> JL Hennessy, DA Patterson Elsevier	<a href="#">18892</a>	2011
<a href="#">Computer Organization and Design ARM Edition: The Hardware Software Interface</a> DA Patterson, JL Hennessy Morgan kaufmann	<a href="#">5242</a>	2016
<a href="#">Memory consistency and event ordering in scalable shared-memory</a>	<a href="#">1726</a>	1990

<u>TITLE</u>	<u>CITED BY</u>	<u>YEAR</u>
<a href="#">multiprocessors</a> K Gharachorloo, D Lenoski, J Laudon, P Gibbons, A Gupta, J Hennessy ACM SIGARCH Computer Architecture News 18 (2SI), 15-26		
<a href="#">The stanford dash multiprocessor</a> D Lenoski, J Laudon, K Gharachorloo, WD Weber, A Gupta, J Hennessy, ... Computer 25 (3), 63-79	<a href="#">1430</a>	1992
<a href="#">The stanford flash multiprocessor</a> J Kuskin, D Ofelt, M Heinrich, J Heinlein, R Simoni, K Gharachorloo, ... Proceedings of 21 International Symposium on Computer Architecture, 302-313	<a href="#">1046</a>	1994
<a href="#">The directory-based cache coherence protocol for the DASH multiprocessor</a> D Lenoski, J Laudon, K Gharachorloo, A Gupta, J Hennessy ACM SIGARCH Computer Architecture News 18 (2SI), 148-159	<a href="#">969</a>	1990
<a href="#">An evaluation of directory schemes for cache coherence</a> A Agarwal, R Simoni, J Hennessy, M Horowitz ACM SIGARCH Computer Architecture News 16 (2), 280-298	<a href="#">817</a>	1988
<a href="#">SUIF: An infrastructure for research on parallelizing and optimizing compilers</a> RP Wilson, RS French, CS Wilson, SP Amarasinghe, JM Anderson, ... ACM Sigplan Notices 29 (12), 31-37	<a href="#">752</a>	1994
<a href="#">The priority-based coloring approach to register allocation</a> FC Chow, JL Hennessy ACM Transactions on Programming Languages and Systems (TOPLAS) 12 (4), 501-536	<a href="#">499</a>	1990
<a href="#">An analytical cache model</a> A Agarwal, J Hennessy, M Horowitz ACM Transactions on Computer Systems (TOCS) 7 (2), 184-215	<a href="#">442</a>	1989
<a href="#">Cache performance of operating system and multiprogramming workloads</a> A Agarwal, J Hennessy, M Horowitz ACM Transactions on Computer Systems (TOCS) 6 (4), 393-431	<a href="#">367</a>	1988
<a href="#">Register allocation by priority-based coloring</a> F Chow, J Hennessy Proceedings of the 1984 SIGPLAN symposium on Compiler construction, 222-232	<a href="#">349</a>	1984
<a href="#">Performance evaluation of memory consistency models for shared-memory multiprocessors</a> K Gharachorloo, A Gupta, J Hennessy ACM SIGPLAN Notices 26 (4), 245-257	<a href="#">344</a>	1991
<a href="#">Load balancing and data locality in adaptive hierarchical N-body methods: Barnes-Hut, fast multipole, and radiosity</a> JP Singh, C Holt, T Totsuka, A Gupta, J Hennessy	<a href="#">329</a>	1995

<u>TITLE</u>	<u>CITED BY</u>	<u>YEAR</u>
Journal of Parallel and Distributed Computing 27 (2), 118-141		
<a href="#">Postpass code optimization of pipeline constraints</a> JL Hennessy, T Gross ACM Transactions on Programming Languages and Systems (TOPLAS) 5 (3), 422-448	<a href="#">328</a>	1983
<a href="#">Two techniques to enhance the performance of memory consistency models</a> K Gharachorloo, A Gupta, JL Hennessy Computer Systems Laboratory, Stanford University	<a href="#">326</a>	1991
<a href="#">Efficient and exact data dependence analysis</a> DE Maydan, JL Hennessy, MS Lam Proceedings of the ACM SIGPLAN 1991 conference on Programming language ...	<a href="#">315</a>	1991
<a href="#">False sharing and spatial locality in multiprocessor caches</a> J Torrellas, HS Lam, JL Hennessy IEEE Transactions on Computers 43 (6), 651-663	<a href="#">310</a>	1994
<a href="#">VLSI processor architecture</a> JL Hennessy IEEE Computer Architecture Letters 33 (12), 1221-1246	<a href="#">305</a>	1984
<a href="#">Comparative evaluation of latency reducing and tolerating techniques</a> A Gupta, J Hennessy, K Gharachorloo, T Mowry, WD Weber Proceedings of the 18th Annual International Symposium on Computer ...	<a href="#">288</a>	1991
<a href="#">The DASH prototype: Implementation and performance</a> D Lenoski, J Laudon, T Joe, D Nakahira, L Stevens, A Gupta, J Hennessy ACM SIGARCH Computer Architecture News 20 (2), 92-103	<a href="#">273</a>	1992
<a href="#">Multiprocessor simulation and tracing using Tango</a> H Davis, SR Goldschmidt, J Hennessy Proceedings of the 1991 International Conference on Parallel Processing 2 ...	<a href="#">269</a>	1991
<a href="#">The DASH prototype: Logic overhead and performance</a> D Lenoski, J Laudon, T Joe, D Nakahira, L Stevens, A Gupta, J Hennessy IEEE Transactions on parallel and distributed systems 4 (1), 41-61	<a href="#">266</a>	1993
<a href="#">Performance tradeoffs in cache design</a> S Przybylski, M Horowitz, J Hennessy [1988] The 15th Annual International Symposium on Computer Architecture ...	<a href="#">224</a>	1988
<a href="#">Compile-time partitioning and scheduling of parallel programs</a> V Sarkar, J Hennessy ACM Sigplan Notices 21 (7), 17-26	<a href="#">221</a>	1986
<a href="#">Hardware/software tradeoffs for increased performance</a> J Hennessy, N Jouppi, F Baskett, T Gross, J Gill ACM SIGPLAN Notices 17 (4), 2-11	<a href="#">218*</a>	1982
<a href="#">Symbolic debugging of optimized code</a>	<a href="#">211</a>	1982



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J Hennessy ACM Transactions on Programming Languages and Systems (TOPLAS) 4 (3), 323-344		
<a href="#">Computer technology and architecture: An evolving interaction</a> JL Hennessy, NP Jouppi Computer 24 (9), 18-29	<a href="#">203</a>	1991
<a href="#">A new golden age for computer architecture</a> JL Hennessy, DA Patterson Communications of the ACM 62 (2), 48-60	<a href="#">197</a>	2019
<a href="#">The future of systems research</a> J Hennessy Computer 32 (8), 27-33	<a href="#">195</a>	1999
<a href="#">Scaling parallel programs for multiprocessors: Methodology and examples</a> JP Singh, JL Hennessy, A Gupta Computer 26 (7), 42-50	<a href="#">190</a>	1993
<a href="#">The performance impact of flexibility in the Stanford FLASH multiprocessor</a> M Heinrich, J Kuskin, D Ofelt, J Heinlein, J Baxter, JP Singh, R Simoni, ... Proceedings of the sixth international conference on Architectural support ...	<a href="#">183</a>	1994
<a href="#">Organização e Projeto de Computadores: a interface hardware/software</a> JL Hennessy, DA Patterson Elsevier Brasil	<a href="#">169</a> *	2014
<a href="#">WSCLOCK—a simple and effective algorithm for virtual memory management</a> RW Carr, JL Hennessy Proceedings of the eighth ACM symposium on Operating systems principles, 87-95	<a href="#">168</a>	1981
<a href="#">Analysis of cache performance for operating systems and multiprogramming</a> A Agarwal, JL Hennessy Kluwer Academic Publishers	<a href="#">166</a>	1989
<a href="#">MIPS: a VLSI processor architecture</a> J Hennessy, N Jouppi, F Baskett, J Gill VLSI Systems and Computations, 337-346	<a href="#">158</a>	1981
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<a href="#">Partitioning parallel programs for macro-dataflow</a> V Sarkar, J Hennessy Proceedings of the 1986 ACM Conference on LISP and Functional Programming ...	<a href="#">153</a>	1986

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<a href="#">Programming for different memory consistency models</a> K Gharachorloo, SV Adve, A Gupta, JL Hennessy, MD Hill Journal of parallel and distributed computing 15 (4), 399-407	<a href="#">141</a>	1992
<a href="#">The accuracy of trace-driven simulations of multiprocessors</a> SR Goldschmidt, JL Hennessy ACM SIGMETRICS Performance Evaluation Review 21 (1), 146-157	<a href="#">140</a>	1993
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<a href="#">SoftFLASH: Analyzing the performance of clustered distributed virtual shared memory</a> A Erlichson, N Nuckolls, G Chesson, J Hennessy ACM SIGPLAN Notices 31 (9), 210-220	<a href="#">137</a>	1996
<a href="#">Optimizing delayed branches</a> TR Gross, JL Hennessy ACM SIGMICRO Newsletter 13 (4), 114-120	<a href="#">136</a>	1982
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<a href="#">Estructura y diseño de computadores</a> DA Patterson, JL Hennessy Reverté	<a href="#">129*</a>	2000
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<a href="#">Shared data placement optimizations to reduce multiprocessor cache miss rates</a> J Torrellas Proceedings of the 1990 International Conference on Parallel Processing, II ...	<a href="#">124</a>	1990

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